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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,419	01/14/2004	Tatsunori Murata	501.43228X00	4551

20457 7590 10/14/2005

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,419	MURATA ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-37 and 42* is/are pending in the application.

4a) Of the above claim(s) *33-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-18,23-32 and 42* is/are rejected.

7)☒ Claim(s) *19-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of 15-32 and 42 in the reply filed on 07 Sept. 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the 'forming a second insulating film to a thickness sufficient to fill a space of the first distance and but not sufficient to fill a space of the second distance', 'etching the second, third and fourth insulating films until the conductive film existing over the side walls of the first semiconductor region of the columnar laminate is exposed', and 'forming a fifth insulating film over the second and third insulating films' must be shown or the feature(s) canceled from the claims 15 and 19-20; no new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 15-18, 23-32, 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 2004/0043550 to Chakihara et al. in view of US 6919237 to Ohtani et al.

Regarding claim 15, Chakihara discloses a method of manufacture of a semiconductor integrated circuit device in fig. 38-47, comprising the steps of:

(a) forming a plurality of columnar laminates P1,P2, fig. 38, having, at the an upper portion and a lower portion thereof, a first semiconductor region 57 and a second semiconductor region 59, respectively, [0222] while spacing the plurality of columnar laminates in a first direction and in a second direction wider than the first direction, fig. 39.

(b) forming conductive films 66 [0225] over the side walls of the columnar laminates via a first insulating film 70 [0238] with a distance, in the first direction, between the conductive films 66 over the side walls of the plurality of columnar laminates P1/P2 as a first distance and with a distance in the second direction as a second distance which is greater than the first distance, fig. 43.

(c) forming a second insulating film 73 [0239] to a thickness sufficient to fill a

space of the first distance and a space of the second distance; and

(d) forming a third insulating film 81 [0244] over the second insulating film and filling the space of the second distance.

But, Chakihara does not disclose forming a second insulating film 73 to a thickness sufficient to fill a space of the first distance and but not sufficient to fill a space of the second distance.

However, Chakihara discloses the method wherein the layer 73 having a general thickness. Accordingly, it would have been obvious to one of ordinary skill in art to use the teaching of Chakihara in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 16, Chakihara discloses a method of manufacture of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a plurality of columnar laminates P1/P2 having, at an upper portion and a lower portion thereof, a first semiconductor region 57 and a second semiconductor region 59, respectively, while spacing the plurality of columnar laminates P1/P2 in a first direction and in a second direction wider than the first direction,

(b) forming conductive films 66 over the side walls of the columnar laminates P1/P2 via a first insulating film 70 with a distance, in the first direction, between

the conductive films over the side walls of the plurality of columnar laminates as a first distance and with a distance in the second direction as a second distance which is greater than the first distance;

(c) depositing a second insulating film 73 between the columnar laminates P1/P2 and thereover with a thickness at least equal to the first distance, and

(d) depositing over the second insulating film a third insulating film 81 with a thickness, after the step (c), between the top of the second insulating film 73 over the second distance portion of the columnar laminates P1/P2 and the top of the second insulating film over the columnar laminates P1/P2.

But, Chakihara does not disclose forming a third insulating film 81 corresponding to at least 70% of a vertical difference.

However, Chakihara discloses the method wherein the layer 81 having a general thickness. Accordingly, it would have been obvious to one of ordinary skill in art to use the teaching of Chakihara in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claims 17-18, 24-25, Chakihara does not disclose a method of manufacture of a semiconductor integrated circuit device wherein the step (c) and step (d) is carried out at a temperature of 700 °C or less, using tetraethoxysilane and ozone as raw materials.

However, Ohtani discloses a method wherein the silicon oxide film 105 or 110 is formed by CVD at about 350-600 oC, using tetraethoxysilane and ozone as raw materials, column 13 lines 34-50 or col. 14 lines 40-46. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use silicon oxide formation teaching of Ohtani with Chakihara's process, because such process is typical in the art

Regarding claim 23, Chakihara does not disclose the method of manufacture of a semiconductor integrated circuit device wherein the second insulating film 73 has better coverage than the third insulating film 81. However, Chakihara discloses a structure that is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claim 26, Chakihara does not disclose the method comprising plasma having a density $10^{11}/cm^2$ or greater.

But Chakihara discloses the method of manufacture of a semiconductor integrated circuit device according to claim 15, wherein the third insulating film 87 is a silicon oxide film [0248] and the step (d) is carried out in a plasma atmosphere having a general plasma concentration. Accordingly, it would have been obvious to one of ordinary skill in art to use the teaching of Chakihara's

method in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Or such conditions are conventional; see also US 6663715 (Yuda) in column 8 lines 28-31.

Regarding claims 27-28, Chakihara does not discloses a method of manufacture of a semiconductor integrated circuit device wherein the columnar laminate has a height of at least 3 times as much as the first distance, wherein the first distance is 150 nm or less and the second distance is 500 nm or greater.

But Chakihara discloses the method of manufacture of a semiconductor integrated circuit device wherein the columnar laminate has a height, wherein the first distance and the second distance having general distance. Accordingly, it would have been obvious to one of ordinary skill in art to use the teaching of Chakihara's method in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claims 29-30, Chakihara discloses the method of manufacture of a semiconductor integrated circuit device wherein the plane pattern of each of the columnar laminate P1/P2 and the conductive film 66 over the side walls thereof is approximately elliptical and a first diameter in the first direction is smaller than a second

diameter in the second direction, wherein the columnar laminate in the step (a) is formed using a mask which is H-shaped in the first direction.

Regarding claims 31-32, Chakihara discloses the method of manufacture of a semiconductor integrated circuit device further comprising, prior to the step (a), the steps of:

(h) forming two pairs of horizontal MISFETS TR1 DR1 having source and drain regions in common, fig. 1 and 47, and

(i) connecting the second semiconductor regions 59 of the two vertical MISFETS adjacent to each other in the first direction to the source and drain regions which the two pairs of horizontal MISFETS have in common, respectively, fig. 1 and 47.

Regarding claim 42, Chakihara discloses a method of manufacture of a semiconductor integrated circuit device wherein the conductive films 66 are formed to encompass the columnar laminates P1/P2.

Allowable Subject Matter

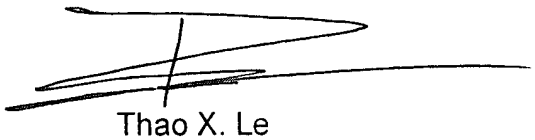
7. Claims 19-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record neither anticipat4ed nor rendered obvious all the limitation of the claims 19-22 including etching the second, third and fourth insulating films until the conductive film existing over the side walls of the first semiconductor region of the columnar laminate is exposed.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le
05 Oct. 2005

Sheet 1 of 1

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO. 501.43228X00	SERIAL NO.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT MURATA, et al.	
		FILING DATE January 14, 2004	GROUP

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
✓	AA	5,198,683	03/30/1993	SIVAN	357	67	05/03/1991
✓	AB	5,670,803	09/23/1997	BEILSTEIN, Jr. et al.	257	278	02/08/1995
✓	AC	5,994,735	11/30/1999	MAEDA, et al.	257	329	11/30/1999
✓	AD	5,627,390	05/06/1997	MAEDA, et al.	257	302	05/06/1997
	AE						
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	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Abstract Yes	Abstract No
✓	AM	11-176936	07/02/1999	JP	H01L	21/768	X	
	AN	9-232447	09/05/1997	JP	H01L	21/8244	X	
	AO	2001-28443	01/30/2001	JP	H01L	29/786	X	
	AP	6-104405	4/15/1994	JP	H01L	27/11	X	
	AQ	03/019663	03/06/2003	WO	H01L	27/11		
✓	AR	00/70683	11/23/2000	WO	H01L	27/108		
	AS							
	AT							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

✓	AU	WATANABE, et al., "A Novel Circuit Technology with Surrounding Gate Transistors (SGT's) for Ultra High Density DRAM's", IEEE Journal of Solid-State Circuits, Vol. 30, No. 9, September 1995
	AV	
	AW	
	AX	
	AY	
	AZ	

Examiner	Date Considered
	07/05/05

Notice of References Cited	Application/Control No. 10/756,419	Applicant(s)/Patent Under Reexamination MURATA ET AL.	
	Examiner Thao X. Le	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-2004/0043550	03-2004	Chakihara et al.	438/199
	B	US-6,919,237	07-2005	Ohtani et al.	438/151
	C	US-6,663,715	12-2003	Yuda et al.	118/723ER
	D	US-2004/0005755	01-2004	Moniwa et al.	438/222
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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	N					
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	P					
	Q					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.